In the Claims:

Claims 1-6 (Canceled).

7. (Currently amended) An integrated search engine device, comprising:

a content addressable memory (CAM) core ~~that is~~ configured to support at least one database of searchable entries therein;

a ~~at least one~~ FIFO memory device ~~that is~~ configured to store addresses of entries that have been aged out of the at least one database and/or entries that have exceeded an activity-based aging threshold; **[[and]]**

a level count register configured to maintain a count of the stored addresses in said a FIFO memory device;

a control circuit ~~that is~~ configured to support automatic generation of an interrupt to an interface of the search engine device and further configured to report ~~reporting of~~ the stored addresses from said ~~at least one~~ FIFO memory device to the **[[an]]** interface ~~of the search engine device~~; and

a level configuration register configured to maintain a threshold count value that specifies how many addresses can be stored in said FIFO memory device before said control circuit automatically generates the interrupt.

8. (Original) The device of Claim 7, wherein said control circuit comprises a first memory device that is configured to store a plurality of age report enable bits that map to respective entries in the at least one database.

Claims 9-13 (Canceled).

14. (Currently amended) An integrated search engine device, comprising:

a content addressable memory (CAM) core ~~that is~~ configured to support at least one database of searchable entries therein; and

a control circuit ~~that is~~ configured to support generation of at least one interrupt to a command host in response to detecting a sufficiently full storage device containing addresses of entries that have been aged out of the at least one database and/or addresses of entries that have exceeded an activity-based aging threshold.

15. (Original) The device of Claim 14, wherein said control circuit is further configured to support reporting of the addresses of the entries from the storage device to the command host, said reporting being programmable on a per entry basis.

16. (Original) The device of Claim 14, wherein the storage device comprises a FIFO memory device.

17. (Currently amended) The device of Claim 16 **[[**10**]]**, wherein said control circuit further comprises:

a level count register ~~that is~~ configured to maintain a count of unreported addresses in said FIFO memory device; and

a level configuration register ~~that is~~ configured to maintain a threshold count value that specifies how many unreported addresses can be stored in said FIFO memory device before said control circuit issues the at least one interrupt.

Claims 18-20 (Canceled).